AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A cascode device structure used for high voltage circuits, the device structure having one or more transistors of a same type connected in a series and being operable with a normal operating voltage and a high operating voltage, the cascode device structure comprising:

a high operating voltage coupled to a first end of the device structure;

a low voltage coupled to a second end; and

one or more control voltages controllably coupled to the gates of the transistors,

wherein at least one of the control voltages coupled to the gate of at least one transistor is raised to a medium voltage level that is substantially higher than a normal operating voltage and lower than the high operating voltage when operating under the high operating voltage for tolerating stress imposed thereon by the high operating voltage.

2. (Original) The structure of claim 1 wherein the medium voltage level is about one half of the high operating voltage.

3. (Currently Amended) The structure of claim 1 wherein the transistors ~~are N type, and the control voltage is coupled to the gate of the transistor that is directly~~

~~coupled to the high operating voltage.~~ comprise a first NMOS transistor directly coupled to the high operating voltage and at least one second NMOS transistor serially coupled between the first NMOS transistor and the low voltage, the control voltage being coupled to a gate of the first NMOS transistor.

4. (Original) The structure of claim 3 wherein the low voltage is a grounding voltage.

5. (Currently Amended) The structure of claim 1 wherein the transistors ~~are P type, and the control voltage is coupled to the gate of the transistor that is directly coupled to the low voltage.~~ comprise a first PMOS transistor directly coupled to the low voltage and at least one second PMOS transistor serially coupled between the first PMOS transistor and the high operating voltage, the control voltage being coupled to a gate of the first PMOS transistor.

6. (Original) The structure of claim 5 wherein the transistors have separated N wells.

7. (Original) The structure of claim 1 wherein the control voltages are determined so that the stress imposed by the high voltage is about equally divided by the transistors in the device structure.

8. (Original) The structure of claim 1 wherein the high operating voltage is above 10V.

9. (Original) The structure of claim 8 wherein the normal operating voltage is below 2V.

10. (Original) The structure of claim 1 wherein the stress is a gated stress.

11. (Original) The structure of claim 1 wherein the stress is a drain stress.

12. (Original-Allowed) A high voltage circuit operating with a normal operating voltage and a high operating voltage, the circuit comprising:

a first cascode device structure having one or more P type transistors connected in series with one end thereof connected to the high operating voltage;

a second cascode device structure in series with the first cascode device structure at its other end having one or more N type transistors; and

one or more control voltages controllably coupled to the gates of the transistors in the first and second cascode device structure for raising voltages on one or more gates of the transistors to one or more medium values that are above the normal operating voltage for tolerating voltage stress imposed by the high operating voltage.

13. (Original-Allowed) The circuit of claim 12 further comprising an input module for passing an input signal for turning on a high voltage output.

14. (Original-Allowed) The circuit of claim 13 wherein the input module has a third cascode device structure with a gate voltage of at least one transistor raised to a medium value.

15. (Original-Allowed) The circuit of claim 13 wherein the control voltages for the first and second cascode device structures are controlled separately depending on the input signal.

16. (Original-Allowed) The circuit of claim 12 wherein the second cascode device structure is further connected to a grounding voltage.

17. (Original-Allowed) The circuit of claim 12 wherein the transistors in the first cascode device structure have separated N wells.

18. (Currently Amended) A high voltage circuit operating with a normal operating voltage and a high operating voltage, the circuit comprising:

a first cascode device structure having one or more P type transistors connected in series with one end thereof connected to the high operating voltage; and

one or more control voltages controllably coupled to the gates of the transistors in the first cascode device structure for raising voltages on one or more gates of the transistors to one or more medium values that are substantially above the normal

operating voltage and below the high operating voltage for tolerating voltage stress imposed by the high operating voltage,

wherein the P type transistors have separated N wells.

19. (Currently Amended) The circuit of claim 18 further comprising a second cascode device structure in series with the first cascode device structure at its other end having one or more N type transistors[[;]].

20. (Original) The circuit of claim 19 wherein the control voltages for the first and second cascode device structures are controlled separately depending on the input signal.

21. (Original) The circuit of claim 19 wherein the second cascode device structure is further connected to a grounding voltage.

22. (Original) The circuit of claim 18 further comprising an input module for passing an input signal for turning on a high voltage output, wherein the input module has an input cascode device structure with a gate voltage of at least one transistor raised to a predetermined medium value.